IN THE CLAIMS

Please amend claims 1 and 7 in the present application. A complete claim listing is provided here for Examiner's convenience:

1. (Currently Amended) A nonplanar semiconductor device comprising:

a semiconductor body having a top surface opposite a bottom surface formed above an insulating substrate, wherein said semiconductor body has a pair of laterally opposite sidewalls;

a gate dielectric formed on said top surface of said semiconductor body, on at least a portion said bottom surface of said semiconductor body, and on said laterally opposite sidewalls of said semiconductor body;

a gate electrode formed on said gate dielectric, on said top surface of said semiconductor body and adjacent to said gate dielectric on said laterally opposite sidewalls of said semiconductor body and beneath said gate dielectric on said bottom surface of said semiconductor body, wherein said gate electrode has a pair of laterally opposite sidewalls oriented perpendicularly to said laterally opposite sidewalls of said semiconductor body, said gate electrode having a top portion and a bottom portion wherein the bottom portion laterally undercuts the top portion at least on said laterally opposite sidewalls of said gate electrode; and

a pair of source/drain regions formed in said semiconductor body on opposite sides of said gate electrode.

2. (Original) The semiconductor device of claim 1 wherein said semiconductor body is a single crystalline silicon film.

3. (Original) The semiconductor device of claim 1 wherein said semiconductor body is selected from the group consisting of germanium, silicon germanium, gallium arsenide, InSb, GaP, GaSb and carbon nanotubes.

4. (Original) The semiconductor device of claim 1 wherein said gate electrode comprises a material selected from the group consisting of polycrystalline silicon, tungsten, tantalum, titanium, and metal nitrides.

5. (Original) The semiconductor device of claim 1 wherein said insulating substrate comprises an oxide film formed on a monocrystalline silicon substrate.

6. (Previously Presented) The semiconductor device of claim 1 wherein said semiconductor device further includes at least one additional semiconductor body having a top surface and a bottom surface, and a pair of laterally opposite sidewalls wherein a gate dielectric layer is formed said top surface, said bottom surface and said sidewalls of said at least one additional semiconductor body, and wherein said gate electrode is formed on said gate dielectric on said top surface of said at least one additional semiconductor body, and adjacent to said gate dielectric on said laterally opposite sidewalls of said at least one additional semiconductor body, and beneath the gate dielectric on said bottom surface of said at least one additional semiconductor body.

7. (Previously Presented) A nonplanar semiconductor device comprising:

a semiconductor body having a top surface opposite a bottom, said semiconductor body having laterally opposite sidewalls formed above said insulating substrate;

a gate dielectric formed on said top surface of said semiconductor body, on said laterally opposite sidewalls of said semiconductor body, and on at least a portion of the bottom surface of said semiconductor body;

a gate electrode formed on said gate dielectric on said top surface of said semiconductor body and adjacent to said gate dielectric on said laterally opposite sidewalls of said semiconductor body, and beneath said gate dielectric on said bottom surface of said semiconductor body, wherein said gate electrode has a pair of laterally opposite sidewalls oriented perpendicularly to said laterally opposite sidewalls of said semiconductor body, wherein said gate electrode has a top portion above said insulating substrate and a bottom portion formed in said insulating substrate wherein said bottom portion ~~is wider~~ has a larger width than said top portion, wherein said width is the dimension of the said gate electrode that is oriented perpendicularly to said pair of laterally opposite sidewalls of said gate electrode; and

a pair of source/drain regions formed in said silicon body on opposite sides of said gate electrode.

8. (Original) The semiconductor device of claim 7 wherein said semiconductor body is a single crystalline silicon film.

9. (Original) The semiconductor device of claim 7 wherein said semiconductor body is selected from the group consisting of germanium, silicon germanium, gallium arsenide, InSb, GaP, GaSb and carbon nanotubes.

10. (Original) The semiconductor device of claim 7 wherein said gate electrode comprises a material selected from the group consisting of polycrystalline silicon, tungsten, tantalum, titanium and metal nitrides.

11. (Original) The semiconductor device of claim 7 wherein said insulating substrate comprises an oxide film formed on a monocrystalline silicon substrate.

12. (Previously Presented) The semiconductor device of claim 7 wherein said semiconductor device further includes at least one additional semiconductor body having a top surface and a bottom surface, and a pair of laterally opposite sidewalls wherein a gate dielectric layer is formed said top surface, said bottom surface and said sidewalls of said at least one additional semiconductor body, and wherein said gate electrode is formed on said gate dielectric on said top surface of said at least one additional semiconductor body, and adjacent to said gate dielectric on said laterally opposite sidewalls of said at least one additional semiconductor body, and beneath the gate dielectric on said bottom surface of said at least one additional semiconductor body.